## HP PDNO 10012382-1 USPTO serial number 10/044,394

## IN THE CLAIM

1	1. (Previously Amended, Currently Amended) A method for managing a memory system
2	having a plurality of subsystems, comprising the steps of:
3	upon accessing the subsystems for a piece of data used by a first process,
4	determining an access time to acquire the piece of data in the
5	memory system;
6	comparing the determined access time to a threshold; and
7	taking an action based on results of the comparing step;
8	wherein
9	a value of the threshold is selected based on whether the value is a
10	realistic time for a memory access;
11	a memory table includes entries pointing to data blocks storing data
12	for at least one subsystem;
13	the entries are used to locate the data stored in the data blocks; and
14	while the first process is being executed, the memory table working
15	with a memory manager managing the data blocks
16	independent of an operating system working with the
17	memory system and independent of a processor working
18	with the memory system.
1	2. (Previously Amended) The method of claim 1 wherein a data block containing the
2	piece of data is placed in the memory system based on information selected in one
3	or a combination of:
4	a movement pattern of data in the data block,
5	a structure of the memory system, and

6	a cache-level architecture in the memory system.
1	3. (Canceled)
1	4. (Canceled)
1	5. (Previously Amended) The method of claim 1 further comprising the steps of:
2	the memory table using a physical address of a memory page
3	corresponding to the piece of data to convert to a location address
4	corresponding to an entry pointing to the location of the piece of
5	data.
1	6. (Previously Amended, Currently Amended) A method for managing a memory system,
2	comprising the steps of:
3	upon accessing the memory system for a piece of data used by a first
4	process,
5	a processor working with the memory system continuing its
6	functions until it is stalled;
7	comparing a time taken to complete the memory access to a
8	threshold; and
9	taking an action based on results of the comparing step; a value of
10	the threshold being selected based on whether the value is a
11	realistic time for a memory access.

1	7. (Original) The method of claim 6 wherein the action is selected in one or a combination
2	of
3	postponing executing the first process and allowing executing a second
4	process;
5	causing the first process to be switched to a second process; and
6	causing a performance monitor on the memory system or on a system
7	using the memory subsystem.
1	8. (Original) The method of claim 6 further comprising the step of polling a latency
2	manager for the time taken to complete the memory access; the latency manger
3	being part of managing the memory system.
1	9. (Previously Amended) The method of claim 6 further comprising the steps of:
2	using a memory table having entries pointing to data blocks storing data
3	for at least one subsystem; and
4	using the entries to locate the data stored in the data blocks.
1	10. (Previously Amended) The method of claim 9 wherein, while the first process is
2	being executed, the memory table working with a memory manager managing the
3	data blocks independent of a processor working with the memory system and
4	independent of an operating system working with the memory system.
1	11. (Previously Amended, Currently Amended) A method for managing a memory
2	system, comprising the steps of:
3	upon accessing the memory system for a piece of data used by a first
4	process

## HP PDNO 10012382-1 USPTO serial number 10/044,394

5	counting a time elapsed from the time the data access starts; the
6	counted time being increased as the data is being accessed;
7	comparing the counted time to a threshold; a value of the threshold
8	is selected based on whether the value is a realistic time for
9	a memory access; and
10	based on results of the comparing step, taking an action selected in
11	one or a combination of
12	postponing executing the first process and allowing
13	executing a second process;
14	causing the first process to be switched to a second process;
15	and
16	causing a performance monitor on the memory system or on
17	a system using the memory system.
1	12. (Previously Amended) The method of claim 11 further comprising the steps of:
2	using a memory table having entries pointing to data blocks storing data
3	for at least one memory subsystem; and
4	using the entries to locate the data stored in the data blocks.
1	13. (Previously Amended, Currently Amended) A computer-readable medium embodying
2	instructions for a computer to perform a method for managing a memory system
3	having a plurality of subsystems, the method comprising the steps of:
4	upon accessing the subsystems for a piece of data used by a first process,
5	determining an access time to acquire the piece of data in the
6	memory system;
7	comparing the determined access time to a threshold; and

8	taking an action based on results of the comparing step;
9	wherein
10	a value of the threshold is selected based on whether the value is a
11	realistic time for a memory access;
12	a memory table includes entries pointing to data blocks storing data
13	for at least one subsystem;
14	the entries are used to locate the data stored in the data blocks; and
15	while the first process is being executed, the memory table working
16	with a memory manager managing the data blocks
17	independent of an operating system working with the
18	memory system and independent of a processor working
19	with the memory system.
1	14. (Previously Amended) The computer-readable medium of claim 13 wherein a data
2	block containing the piece of data is placed in the memory system based on
3	information selected in one or a combination of:
4	a movement pattern of data in the data block,
5	a structure of the memory system, and
6	a cache-level architecture in the memory system.
1	15. (Canceled)
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1.	16. (Canceled)
1	17. (Previously Amended) The computer-readable medium of claim 13 wherein the
2	method further comprises the steps of:

3	the memory table using a physical address of a memory page
4	corresponding to the piece of data to convert to a location address
5	corresponding to an entry pointing to the location of the piece of
6	data.
1	18. (Previously Amended, Currently Amended) A computer-readable medium embodying
2	instructions for a computer to perform a method for managing a memory system,
3	the method comprising the steps of:
4	upon accessing the memory system for a piece of data used by a first
5	process,
6	a processor working with the memory system continuing its
7	functions until it is stalled;
8	comparing a time taken to complete the memory access to a
9	threshold; a value of the threshold being selected based on
10	whether the value is a realistic time for a memory access;
11	and
12	based on results of the comparing step, taking an action.
1	19. (Original) The computer-readable medium of claim 18 wherein the method further
2	comprises the step of polling a latency manager for the time taken to complete the
3	memory access; the latency manger being part of managing the memory system.
1	20. (Previously Amended) The computer-readable medium of claim 18 wherein the
2	method further comprises the steps of:
3	using a memory table having entries pointing to data blocks storing data
4	for at least one subsystem; and

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1	21. (Previously Amended, Currently Amended) A computer-readable medium
2	embodying instructions for a computer to perform a method for managing a
3	memory system, the method comprising the steps of:
4	upon accessing the memory system for a piece of data used by a first
5	process,
6	counting a time elapsed from the time the data access starts; the
7.	counted time being increased as the data is being accessed;
8	comparing the counted time to a threshold, a value of the threshold
9	being selected based on whether the value is a realistic time
10	for a memory access; and
11	based on results of the comparing step, taking an action selected in
12	one or a combination of
13	postponing executing the first process and allowing
14	executing a second process;
15	causing the first process to be switched to a second process;
16	and
17	causing a performance monitor on the memory system or on
18	a system using the memory subsystem.
1	22. (Previously Amended) The computer-readable medium of claim 21 wherein the
2	method further comprises the steps of:
3	using a memory table having entries pointing to data blocks storing data
4	for at least one memory subsystem; and
5	using the entries to locate the data stored in the data blcoks.

1	23. (Previously Amended, Currently Amended) An apparatus for managing a memory
2	system having a plurality of subsystems, comprising:
3	means for, upon accessing the subsystems for a piece of data used by a first
4	process,
5	determining an access time to acquire the piece of data in the
6	memory system;
7	comparing the determined access time to a threshold; and
8	taking an action based on results of the comparing step;
9	wherein
10	a value of the threshold is selected based on whether the value is a
11	realistic time for a memory access;
12	a memory table includes entries pointing to data blocks storing data
13	for at least one subsystem;
14	the entries are used to locate the data stored in the data blocks; and
15	while the first process is being executed, the memory table working
16	with a memory manager managing the data blocks
17	independent of an operating system working with the
18	memory system and independent of a processor working
19	with the memory system.
1	24. (Previously Amended) The apparatus of claim 23 wherein a data block containing the
2	piece of data is placed in the memory system based on information selected in one
3	or a combination of:
4	a movement pattern of data in the data block,
5	a structure of the memory system, and
6	a cache-level architecture in the memory system.

1	25. (Canceled)
1	26. (Canceled)
1	27. (Previously Amended) The apparatus of claim 23 wherein the memory table using a
2	physical address of a memory page corresponding to the piece of data to convert to
3	a location address corresponding to an entry pointing to the location of the piece of
4	data.
1	28. (Previously Amended, Currently Amended) An apparatus for managing a memory
2	system, comprising:
3	upon accessing the memory system for a piece of data used by a first
4	process,
5	a processor for working with the memory system and for
6	continuing its functions until it is stalled;
7	means for comparing a time taken to complete the memory access
8	to a threshold; a value of the threshold being selected based
9	on whether the value is a realistic time for a memory access;
10	and
11	means for taking an action based on results of comparing.
1	29. (Original) The apparatus of claim 28 further comprising means for polling a latency
2	manager for the time taken to complete the memory access; the latency manger
3	being part of managing the memory system.

1	30. (Previously Amended) The apparatus of claim 28 further comprising a memory table
2	having entries pointing to data blocks storing data for at least one subsystem; the
3	entries being used to locate the data stored in the data blocks.
1	31. (Previously Amended, Currently Amended) An apparatus for managing a memory
2	system, comprising:
3	upon accessing the memory system for a piece of data used by a first
4	process,
5	means for counting a time elapsed from the time the data access
6	starts; the counted time being increased as the data is being
7	accessed;
8	means for comparing the counted time to a threshold, a value of the
9	threshold being selected based on whether the value is a
10	realistic time for a memory access; and
11	means for taking an action selected in one or a combination of
12	postponing executing the first process and allowing
13	executing a second process;
14	causing the first process to be switched to a second process;
15	and
16	causing a performance monitor on the memory system or on
17	a system using the memory subsystem.
1	32. (Previously Amended) The apparatus of claim 31 further comprising a memory table
2	having entries pointing to data blocks storing data for at least one memory
3	subsystem; the entries being used to locate the data stored in the data blocks.

- 1 33. (Previously Presented) The method of claim 5 wherein the physical address of the
- 2 memory page is converted from a virtual address of the piece of data.
- 1 34. (Previously Presented) The computer-readable medium of claim 17 wherein the
- 2 physical address of the memory page is converted from a virtual address of the
- 3 piece of data.
- 1 35. (Previously Presented) The apparatus of claim 27 wherein the physical address of the
- 2 memory page is converted from a virtual address of the piece of data.